NEW TOPOLOGY OF THE GaAs NON-LINEAR TRANSMISSION LINE (NLTL) USING MICROSTRIP LINE TECHNOLOGY

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ABSTRACT

A novel NLTL is designed using microstrip as an alternative to the coplanar wave guide (CPW) approach which has the advantage of reduced chip size and cost. A frequency multiplier has been designed with the number of sections optimized for power output using harmonic balance simulation. The large and small signal models of the 4*75 μm GaAs schottky diode which is used in the design are verified using S-parameters and large signal measurements.

INTRODUCTION

The NLTL is a monolithic circuit which typically consists of CPW connected in shunt with reverse bias schottky diodes acting as voltage variable capacitors[1],[2]. The primary application of the NLTL is in sampling circuits where it is used as a harmonic and pulse generator[2]. The performance of the NLTL is determined by the cut off frequency of the schottky diode and the skin effect losses[1]. To function properly in a NLTL the schottky diode should have small series resistance and a highly nonlinear CV characteristics. High non-linearity of the schottky diode can be achieved by using an exponentially graded doping profile[3]. Pulse signals can be generated by tapering exponentially the per section cutoff frequency[2],[4]. CPW is commonly used in the NLTL with the advantage that both signal and ground metalization are on the same plane which makes diode grounding very easy. The disadvantage of the CPW is that it occupies significant GaAs MMIC real estate and consequently has high cost. In this paper the technology of the microstrip line and via holes is utilized. The advantage of using microstrip line is that a zigzag path is easily realized to reduce the chip size however a via hole is needed to ground each diode. The GMMT model for the via hole (valid up to 20 GHz) is used in the simulation.

DESIGN CONSIDERATION

The 4*75 μm GaAs schottky diode is selected from the GMMT F20 MMIC process which has the following capacitance voltage characteristics (GMMT model)[5]

$$c_j(v) = \frac{0.377}{(1 - v/1.1)^{0.76}} \qquad (1)$$

The 4*75 μm schottky diode fabricated using the GMMT foundry is pictured in figure 1. S-parameter measurements were performed for the range of bias points (0 , -8V) to verify the GMMT model. Figure 2 shows the measured and simulated (GMMT model) S-parameters for the 0,-5V bias points were in good agreement. The measured and modeled fundamental and second harmonic are shown in figures 3,4 for bias points -2,-1V. To assure good transmission the large

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signal input impedance(Z_l)should be equal to 50Ω where[2]

$$Z_l = \sqrt{\frac{L_o}{C_o + C_l}} \qquad (2)$$

L_o, C_o are the per section inductance and capacitance of the microstrip line. C_l is the large signal capacitance of the diode which is given by

$$C_l = C_{coupling} + \frac{1}{v_{high} - v_{low}} \int_{v_{low}}^{v_{high}} C_j(v)dv \qquad (3)$$

C_l is computed to be 0.15 pF. The diode large signal capacitance should dominate over the microstrip line capacitance, this requires that $Z_o \geq 75\Omega$ [2], Z_o is set to 100 Ω which corresponds to a microstrip line width of 16 μm (computed using the GMMT model). The length per section of the microstrip line is designed to be 670 μm to realize a 50 Ω large signal input impedance. The microstrip line is bent by 90° as shown in figure 5 in order to compress the chip size. The effect of 90° bends and the tee junctions is taken into account using frequency dependent discontinuity models.

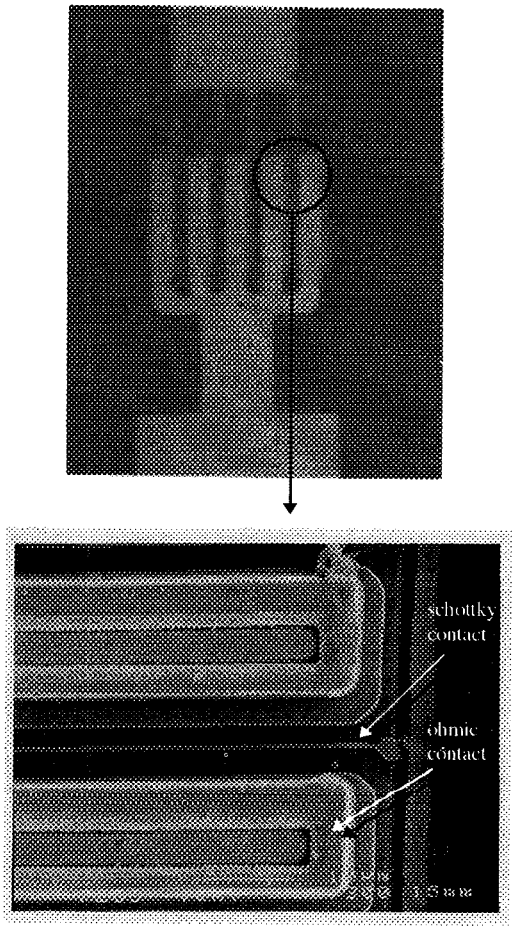


Figure 1 Photograph of the 4*75 μm Schottky diode (GMMT foundry).

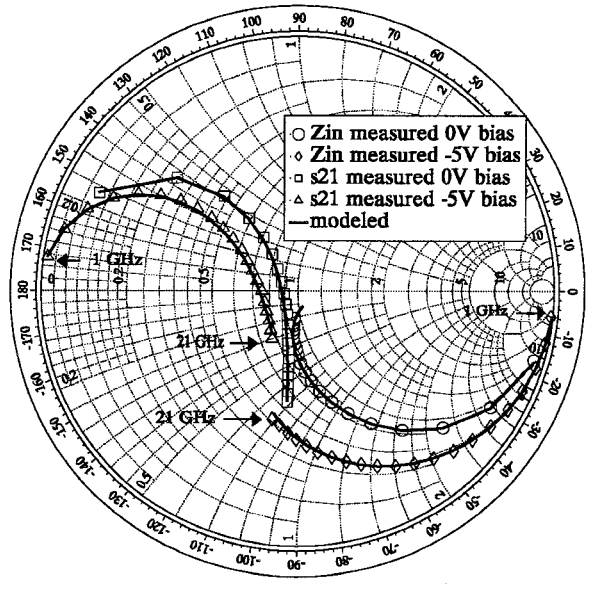


Figure 2 Measured and modeled transmission coefficient (S_{21}) and input impedance (Zin, normalized by 50Ω) for the 4*75μm schottky diode, the frequency range is (1-21 Ghz).

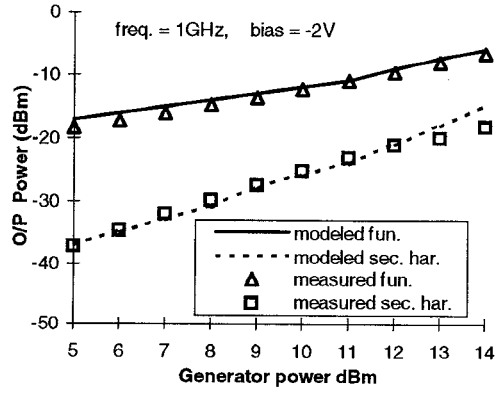


Figure 3 Measured and modeled output fundamental and second harmonic versus the generator power in dBm for -2V bias.

SIMULATION RESULTS

The electrical model of the designed structure is constructed using the GMMT models of the individual components (microstrip lines, corners, tee junctions, via holes and schottky diodes). The MDS harmonic balance simulator is used to run the simulation. Figure 6 shows the maximum second order harmonic power as a function of the number of sections for 20 dBm input power with a -2.5V bias. In figure 6 as the number of sections is increased the maximum second order harmonic power increases up to 8 sections beyond that the maximum second order harmonic power begins to decrease slowly.

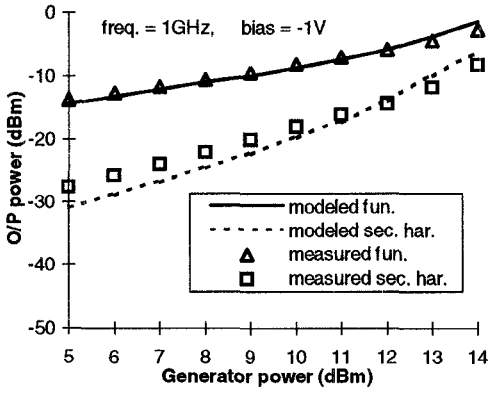
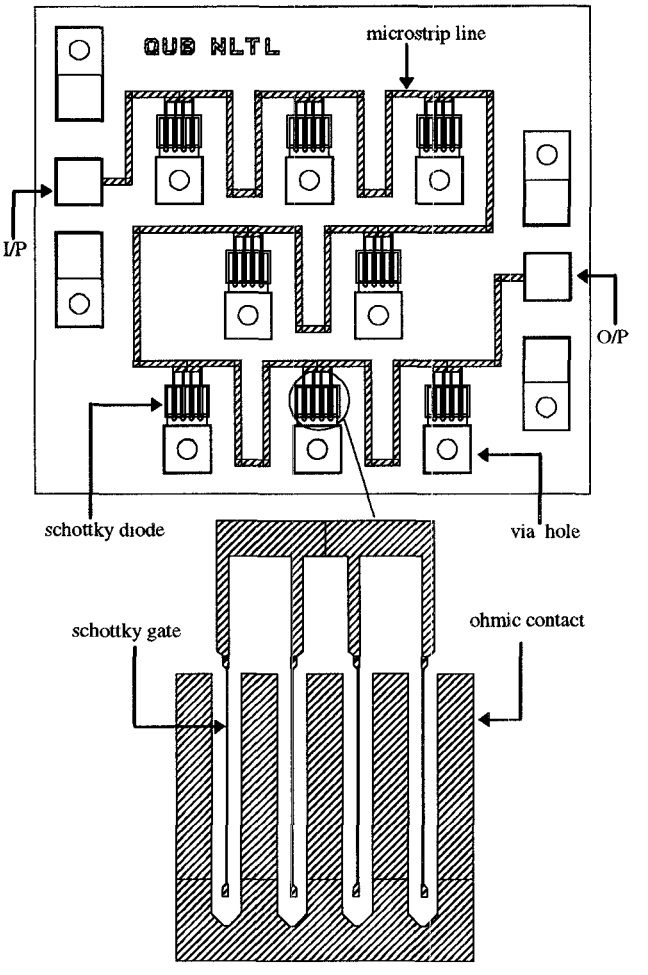
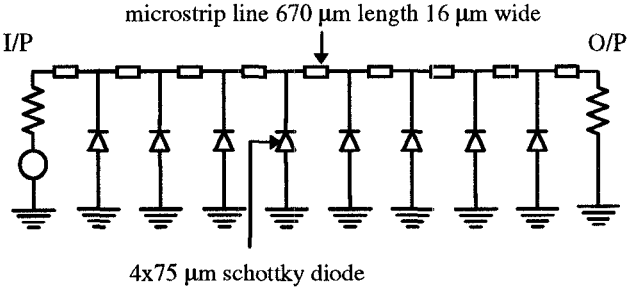


Figure 4 Measured and modeled output fundamental and second harmonic versus the generator power in dBm for -1V bias.

This occurs because after 8 sections the power transferred from the fundamental to the second harmonic becomes less than the power lost through the NLTL. Larger maximum second order harmonic power could be achieved by decreasing the losses and increasing the number of sections. Figure 7 shows a comparison of results for 8,16,24 section NLTLs. As the number of sections becomes larger the cut off frequency begins to decrease and the power curve becomes more flattened. Figure 8 shows the output power of the fundamental, second and third harmonics as a function of the input frequency for 20 dBm input signal power, these results are similar to the results obtained by Rodwell [2] for a CPW based NLTL.



(a)



(b)

Figure 5 (a)Layout of the designed NLTL chip (b) Schematic diagram.

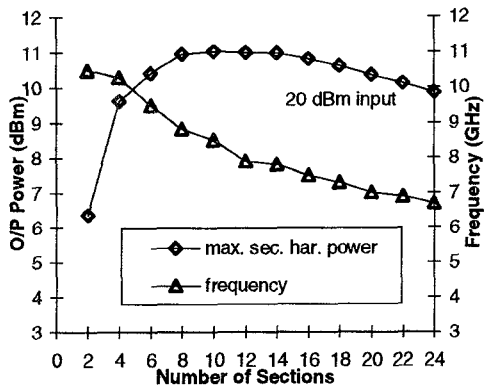


Figure 6 Simulated maximum second harmonic power and the corresponding frequency versus number of sections.

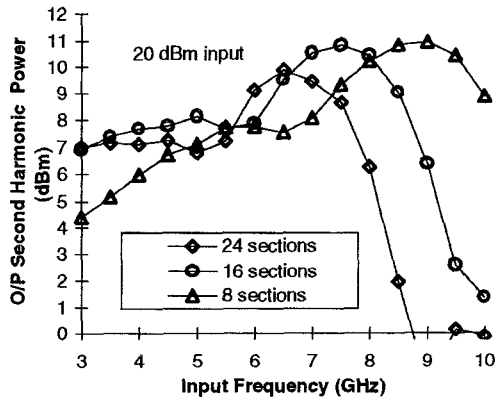


Figure 7 Simulated second harmonic output power versus frequency for 8, 16, 24 section NLTL.

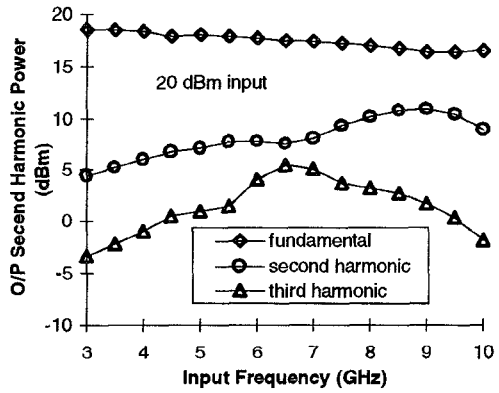


Figure 8 Simulated fundamental, second and third harmonics power versus frequency for 20 dBm input power (8 sections)

CONCLUSION

Via holes and microstrip line technology are used as an alternative to CPW in the construction of the NLTL. A NLTL with compressed chip size has been designed and simulated based on the new technology. The number of sections has been optimized using electrical models based on harmonic balance simulation.

ACKNOWLEDGMENT

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